

Stallcup S Electrical Design 2008 Edition

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Power Integrity for Nanoscale Integrated Systems
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proven methods for noise tolerant nanoscale integrated circuit design this leading edge guide discusses the impact of power integrity from a design perspective emphasizing phenomena and problems induced by power integrity degradation and the latest design trends including low power design power integrity for

nanoscale integrated systems describes how these problems can be forecast early in the design process and the countermeasures that can be used to address them such as the inclusion of inductance and accurate modeling for pi analysis as well as robust circuit design detailed examples and a case study on the ibm power7 processor illustrate real world applications of the techniques presented in this practical resource coverage includes significance of power integrity for integrated circuits supply and substrate noise impact on circuits clock generation and distribution with power integrity signal and power integrity design for i o circuits power integrity degradation and modeling lumped distributed and 3d modeling for power integrity chip temperature and pi impact low power techniques and pi impact power integrity case study using the ibm power7 processor chip carbon nanotube interconnects for power delivery

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